An RCC Receiver IC with TAD-DQD and ADPLL Using Frequency Multiplying Number with Decimals

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***Abstract*—A 0.18-µm CMOS RCC (radio-controlled clock) receiver IC with TAD (Time A/D converter) and ADPLL was realized. This IC, which receives low-frequency (LF) standard time waves, performs AM detection with digital circuits. It has two key components. First, TAD is an all-digital analog-to-digital converter, whose voltage resolution is settable (15µV/LSB at 100kS/s and 3.1mV/LSB at 20MS/s). Second, the ADPLL applying a frequency multiplying number of 4.8828125 generates a 160 kHz ADC (TAD) sampling clock from a 32.768 kHz quartz-clock for digital detection processing. The DSP section, which operates as an adder-subtractor and digital filters, consists of standard cells (75,000 gates). This test IC achieved minimum detectable sensitivity of 0.7 µVrms and maximum detectable sensitivity of 100 mVrms for a standard time wave of 40 kHz at the LNA input terminal. Since the TAD sampling frequencies are settable with desirable multiplying numbers with decimals, the IC can receive different kinds of LF standard time waves such as 40 kHz (JP), 60 kHz (JP), 77.5 kHz (DE), and 68.5 kHz (CN) without any use of quartz-crystal filters.**

I. INTRODUCTION

In recent years, radio-controlled clocks/watches that receive low-frequency (LF) standard time waves, such as the DCF77 (77.5 kHz: Germany) [1], the WWVF (60 kHz: US) [2], the JJY (40 and 60 kHz: Japan) [3], and the BPC (68.5 kHz: CN) [4], have become common. Conventional radio-controlled clocks/watches, however, generally employ analog receiver circuits including quartz-crystal filters and some passive parts such as resistors and capacitors [5], which have to be located outside of an analog-type receiver IC. Such a configuration leads to problems of cost and space (size). Hence, we report a radio-controlled clock (RCC) receiver IC that performs low-frequency AM detection with almost entirely digital circuitry without outside parts except an antenna.

In order to achieve our new receiver prototype IC, we use two original methods: 1) the TAD-DQD (TAD Digital-Quadrature-Detection) [6], and 2) the ADPLL (All-Digital PLL) using a frequency multiplying number with decimals [7]. As for digital quadrature detection, the Time Analog-to-Digital converter (TAD) [8]–[10] has features not found in conventional analog-to-digital converters (ADCs), including an all-digital and small-scale configuration, and continuous integration of input voltage Vin without any dead time. First, we briefly explain TAD-DQD using these effects. Also a newly developed 0.18-µm CMOS TAD is described. By performing simple digital calculations on the A/D converted value, TAD-DQD detects the amplitude and phase from a specific frequency carrier wave [6]. This method requires ADC (TAD) sampling clocks which are fourfold frequency clocks against carrier frequencies (*fcar*) such as 40 kHz, 60 kHz, 77.5 kHz and 68.5 kHz, respectively.

Next, we describe our ADPLL [7] to produce the ADC sampling clocks from the 32.768 kHz reference clock, which has usually been used for conventional quartz watches/clocks. Obviously, it is very reasonable to employ the 32.768 kHz clock as a reference to reduce product cost and space, but in this case we cannot use traditional PLLs including [11] as a frequency multiplier since the required frequency multiplying numbers are not integral to achieve fourfold frequency clocks (160 kHz, 240 kHz, 310 KHz, and 274 kHz) against carrier frequencies (*fcar* = 40 kHz, 60 kHz, 77.5 kHz and 68.5 kHz) from the 32.768 kHz reference clock. Thus, the ADPLL [7] must be employed both to produce the ADC sampling clocks and be embedded on the digital-rich IC chip with the TAD-DQD method.

In this paper, Section II briefly discusses the principles of the TAD-DQD, and Section III will explain the 0.18-µm TAD basic operations. Section IV shows the ADPLL operation for the RCC receiver circuit. Next, the RCC receiver IC configuration and experimental results are shown in Section V. Finally, some conclusions are presented in Section VI.

II. PRINCIPLES OF TAD-DQD

This section describes the proposed principle of TAD-DQD [6] in Fig. 1. In this method the ADC (TAD) sampling frequency (*fs*) should be set at 4·*fcar*. Symbols [a], [b], [c], and [d] are shown as respective area datum for each hatching region. Since TAD output data indicate moving-average results for the Vin levels for the A/D conversion period *Ts* [8], "Calculation: + [a] − [b] − [c] + [d]" gives *Ic* as the "In-phase

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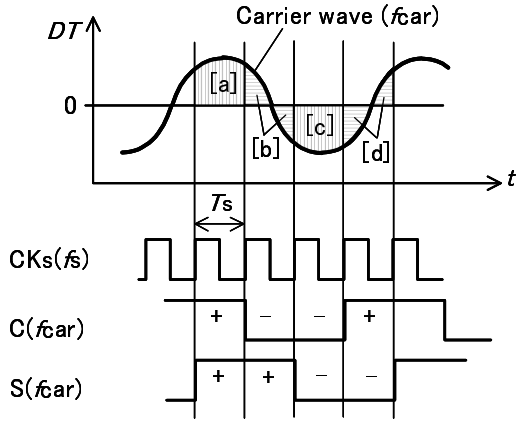

Fig. 1. Digital quadrature detection method.

component," and "Calculation: + [a] + [b] − [c] − [d]" gives *Qc* as the "Quadrature phase component," as shown in Fig. 1. Therefore, the information for carrier waveform amplitude *Am* can be obtained by calculating the square root of ($Ic^2 + Qc^2$), and the information for carrier waveform phase ϕ can be understood by computing arg(*Qc*/*Ic*).

III. TAD Basic Operation

As shown in Fig. 2, TAD is an all-digital A/D converter including a ring-delay-line (RDL) as *the pulse delay line* with 32 delay units (32 DUs) (DU = 2 inverters), along with a 20-bit RDL frequency counter, latch and encoder. The operation principle is described in [8]–[10]. Data on the difference between successive data from the latches are output as 25-bit DT conversion data coinciding with CKs. Sample holds are unnecessary, and a low-pass filter function (defined as TAD filter effect in [8]), which consists of analog moving-average processing, removes any high-frequency noise on the Vin signal, such as clock noises, thermal noises, and RDL delay unit switching noises, simultaneously with A/D conversion. Since its cut-off frequency (*fcut*) is always theoretically equal to 0.443·*fs*, suitable noise reduction can be achieved for any A/D conversion rate including the TAD-DQD method.

Figure 3 shows a 25-bit TAD photomicrograph with 0.044 mm^2 in a 0.18-μm digital CMOS, as compared with 0.45 mm^2 for a 0.8-μm CMOS 18-bit TAD [8]. Since there are few delay units in the RDL, the area voltage-modulated by the input voltage Vin can be extremely small, so as to closely match the mutual characteristics of the DUs.

As an example, the A/D conversion characteristics at 100 kS/s (25ºC) are shown in Fig. 4. Approximately 28000 to 80000 digital values correspond to an A/D conversion range of 1.0 to 1.8 V of a Vin span of 800 mV, with the change component 52000. Accordingly, the voltage resolution is around 15.7-bit at 15 μV/LSB. The power consumption is 1.3 mW from a 1.8 V supply voltage. Non-linearity is ±1.15% FS per 800 mV span. However, if necessary, non-linearity errors can be easily compensated for by digital processing [9], [10] with 10–20 thousand gates using reference points, resulting in ±0.3% FS. Next, the A/D conversion characteristics at 20 MS/s with 1.7 mW are shown in Fig. 5. The voltage resolution is 8-bit at 3.1 mV/LSB, since the sampling period *Ts* (50 ns) is

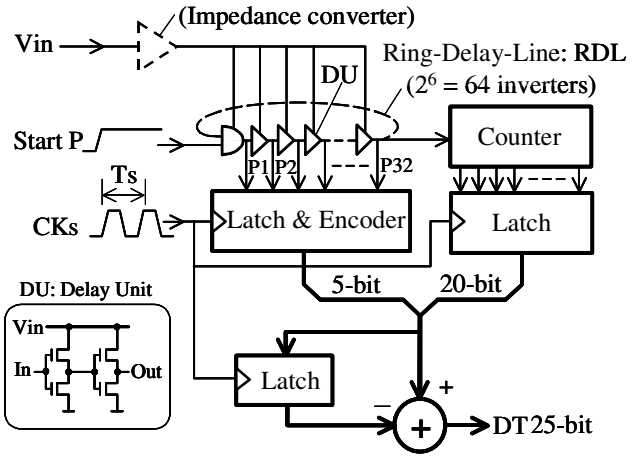

Fig. 2. Block diagram of the ADC (TAD).

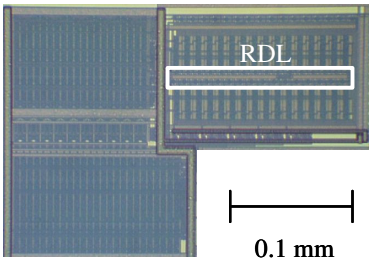

Fig. 3. Photomicrograph of TAD-IC core.

200 times shorter than 10 μs (100 kS/s) in Fig. 4. In this way, TAD can operate in a wide range of 100 k to 20 MS/s. Hence, we can use desirable frequencies for RCC receiver including

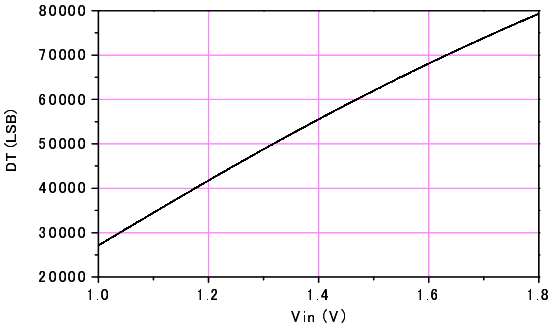

Fig. 4. Characteristics of A/D conversion, fs = 100 kHz.

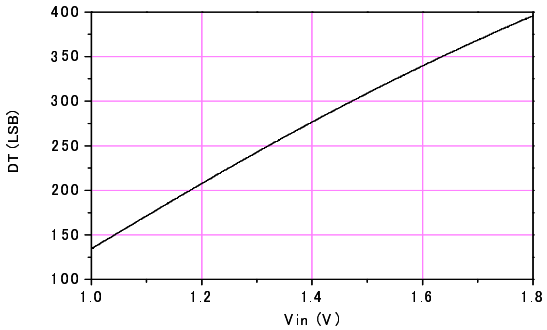

Fig. 5. Characteristics of A/D conversion, fs = 20 MHz.

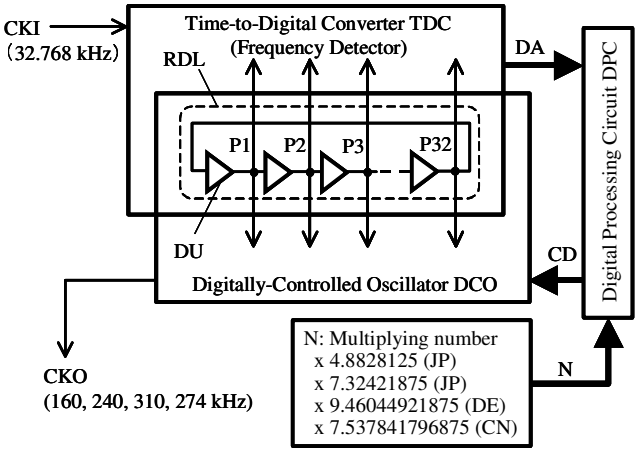

Fig. 6. Block diagram of all-digital PLL with RDL.

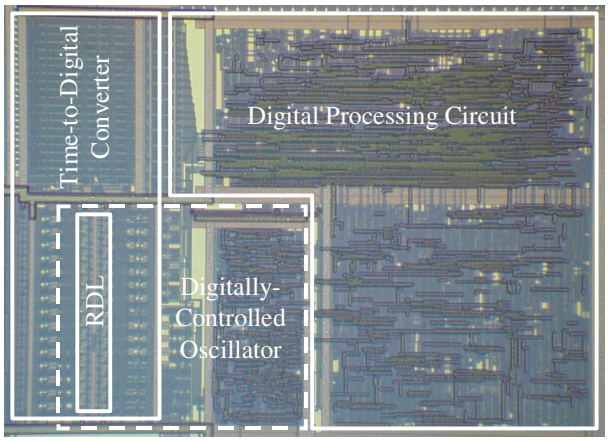

Fig. 7. Photomicrograph of the ADPLL core.

160 kHz sampling, 240 kHz, 310 kHz, and 274 kHz.

Voltage resolution density drift was around -8%, +8% against 25ºC changes in a temperature range of -30–85ºC, but this can also be resolved by digital calculation correction to obtain the ratio to reference voltage values. In TAD-DQD the compensation for the drift and non-linearity is not necessary, since their levels are low enough for the digital detection.

IV. ADPLL Operation for RCC-Receiver IC

In the method of applying the ADPLL [7] for an RCC receiver circuit, as mentioned in Section I, we must employ a frequency multiplying number with decimals to produce an ADC sampling clock with 160 kHz against a 40 kHz low-frequency (LF) standard time wave, for example. In this case, the frequency multiplying number should be 4.8828125.

The block configuration of an all-digital PLL is shown in Fig. 6. This method uses a time-to-digital converter (TDC) with the same architecture as TAD [8] with a fixed Vin as a frequency detector, a digitally-controlled oscillator (DCO) as a frequency variable oscillator, and a digital processing circuit (DPC). The time resolution of both circuits TDC and DCO is determined by a common ring-delay-line (RDL), so that the time resolution is always the same as the gate delay time *Td* of a delay unit DU consisting of two inverters. This ensures that both have the same time resolution even with temperature fluctuations or process variations. Taking advantage of this characteristic, frequency multiplication using numbers *N* with decimals is possible. In this study *N* is settable, for instance, *N* = 4.8828125 (40 kHz), 7.32421875 (60 kHz), 9.46044921875 (77.5 kHz), and 7.537841796875 (68.5 kHz), respectively. In Fig. 6 DA indicates the time interval digital data of one CKI (input reference clock) period and CD represents the number of DUs for one CKO (multiplied output clock) period.

For the frequency acquisition, first, with the gate delay time *Td* (~1.3 ns, 0.69 V-VDD) of the DU as the time resolution, one period of the reference clock CKI (32.768 kHz) receiving external input is digitized (DA = *n*) by the time-to-digital converter. Next, the ratio of this data DA and the frequency multiplying factor *N* (4.8828125) with decimals is calculated in the digital processing circuit (DPC), and the output clock control data CD is generated (CD = *n*/*N*). Then, an output clock CKO (160 kHz) with a period corresponding to this control data CD is generated. With these operations, the

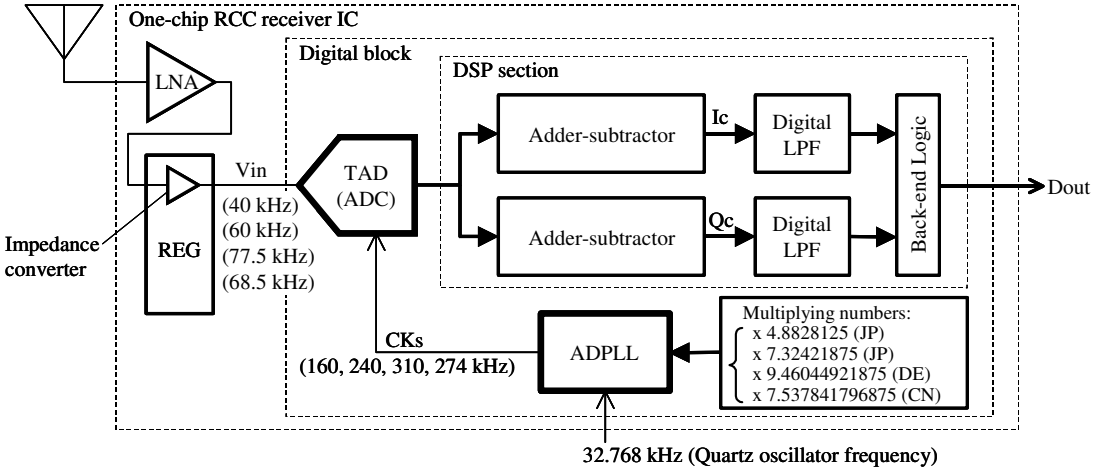

Fig. 8. Radio-Controlled Clock (RCC) receiver circuit block diagram.

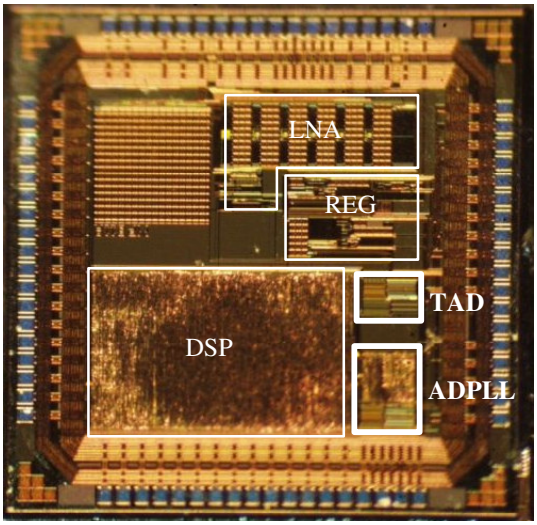

Fig. 9. Photomicrograph of RCC receiver IC chip (2.5 mm x 2.5 mm).

frequency acquisition is complete and repeated with strictly digital processing. Figure 7 shows a photomicrograph of the ADPLL active area measuring 370 μm x 260 μm (0.096 mm^2). Detailed descriptions of the ADPLL are given in [7].

V. IC Configuration and Experimental Results

One prototype receiver method is shown as a Radio-Controlled Clock (RCC) receiver circuit block diagram in Fig. 8, which includes an LNA with AGC (automatic gain control), regulator (REG), 15-bit TAD, DSP section and the ADPLL. In this study the Vin signal frequency is 40 kHz (standard time wave: JJY). Accordingly, the ADC (TAD) sampling clock frequency *fs* should be 160 kHz (4 x 40 kHz), which is generated from the external 32.768 kHz crystal oscillator clock using the ADPLL [7]. After ADC (TAD), the information for both *Ic* and *Qc* can be obtained digitally by applying the calculations mentioned in Section II in the DSP section [6]. The DSP section also performs digital low-pass filters and has a time code generator in the back-end logic section.

Next, a one-chip RCC receiver test IC was shown in Fig. 9. This IC was fabricated with 0.18-μm CMOS with a chip size of 6.25 mm^2. The LNA and the REG are designed with conventional op-amps. An impedance converter for TAD Vin terminal to drive the RDL circuit is included in the REG section. The impedance converter is made of a small-sized op-amp (45 μm x 50 μm). TAD does not need any high-speed op-amp to drive the RDL as the impedance converter, since the TAD filter effect [8] can eliminate RDL switching noises. In this IC, the Vin voltage level for TAD input is very low, ranging from 0.6 V to 0.8V to reduce the power consumption as well as the ADPLL. The DSP section consists of standard cells (75000 gates). This test IC achieved a minimum detectable sensitivity of 0.7 μVrms and a maximum detectable sensitivity of 100 mVrms for a standard time wave of 40 kHz at the LNA input terminal. This experimental result is almost the same as conventional analog type receiver performance, without the use of outside parts, either quartz-crystal filters or passive parts. In addition, regarding reception results of the other low-frequency (LF) standard time waves such as 60 kHz (JP) and 77.5 kHz (DE) except 68.5 kHz (CN), we also experimentally confirmed the minimum detectable sensitivities of 0.9 μVrms and 1.6 μVrms, respectively.

The total IC consumption current is 260 μA, including extra current from evaluation circuits. Hence, it is possible to reduce the consumption current to the same or less than that of conventional analog type receivers by optimizing the IC design. Also, the chip size can be decreased to 4.0 mm^2 to remove evaluation circuits as well. In addition, since the digital block occupies an active area of more than 60% of the IC total area, it can be very effective to apply the shrink process to reduce power consumption much more as well as the chip size.

VI. Conclusion

We have developed the TAD-DQD one-chip receiver IC with the newly designed TAD and the ADPLL using a frequency multiplying number with decimals. This is a prototype IC for a Radio-Controlled Clock (RCC) receiver with 0.18-μm CMOS. The IC achieved a minimum detectable sensitivity of 0.7 μVrms for a 40 kHz standard time wave (JJY) without quartz-crystal filters or passive parts such as resistors and capacitors with a low supply voltage. This prototype IC can also receive other standard time waves such as 60 kHz (JP), 77.5 kHz (DE), and 68.5 kHz (CN) as well, using desirable frequency multiplying numbers.

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